

CLAIMS

What is claimed is:

- Sub A1
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1. A method for erasing a semiconductor device comprising:
applying a voltage pulse at the source of the semiconductor device;
and
applying a multiple step voltage pulse of the opposite polarity, said
multiple voltage pulse having at least a first voltage pulse and a second
voltage pulse, at the gate of the semiconductor device;
10 wherein said second voltage pulse is greater in magnitude than said
first voltage pulse.
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2. The method of claim 1, wherein the multiple step voltage pulse
comprises:
applying the first voltage pulse for a first time interval; and
applying the second voltage pulse for a second time interval;
wherein the first and second time intervals are substantially
coincidental with applying the voltage pulse at the source of the
semiconductor device
20
3. The method of claim 1, wherein the voltage pulse at the source of the
semiconductor device is between about 4.0 V and about 6.0 V.
- 25
4. The method of claim 1, wherein the voltage pulse at the source of the
semiconductor device is about 5.0 V.
5. The method of claim 1, wherein the voltage pulse further comprises
applying the voltage pulse for a third time interval.
- Sub A2

6. The method of claim 5, wherein the third time interval is between about 100 μ sec and about 100 msec.

7. The method of claim 5, wherein the third time interval is about 500 μ sec.

8. The method of claim 1, wherein the first voltage pulse is between about -4.0 V and about -6.0 V. ©

9. The method of claim 1, wherein the first voltage pulse is about -5.0 V.

10. The method of claim 1, wherein the second voltage pulse is between about -9.0 V and about -11.0 V.

11. The method of claim 1, wherein the second voltage pulse is about -10.0 V.

12. The method of claim 2, wherein the first time interval is between about 250 μ sec and about 500 μ sec.

13. The method of claim 2, wherein the first time interval is about 300 μ sec.

14. The method of claim 2, wherein the second time interval is between about 100 μ sec and about 300 μ sec.

15. The method of claim 2, wherein the second time interval is about 200 μ sec.

16. The method of claim 1, wherein the voltage pulse at the source of the semiconductor device further comprises:

applying a third voltage pulse for a first time interval; and
applying a substantially identical fourth voltage pulse for a second
time interval;

wherein the first time interval and the second time interval are
separated by a third time interval during which no voltage pulse is applied to
the source of the semiconductor device.

17. The method of claim 16, wherein the third voltage pulse and the fourth
voltage pulse are about 5.0 V.

18. The method of claim 16, wherein the first time interval is substantially
identical to the second time interval.

19. The method of claim 16, wherein the first time interval and the second
time interval are greater than the third time interval.

20. The method of claim 16, wherein the first time interval is between
about 100 μ sec and about 300 μ sec, the second time interval is between about
10 μ sec and about 30 μ sec and the third time interval is between about 100
 μ sec and about 300 μ sec.

21. The method of claim 16, wherein the first time interval is about 200
 μ sec, the second time interval is about 20 μ sec and the third time interval is
about 200 μ sec.

22. The method of claim 16, wherein the multiple step pulse at the gate of
the semiconductor device comprises:

applying the first voltage pulse for a fourth time interval; and
applying the second voltage pulse for a fifth time interval;

wherein the first voltage pulse and the second voltage pulse are separated by a sixth time interval during which no voltage pulse is applied to the gate of the semiconductor device.

5 23. The method of claim 22, wherein the first voltage pulse is about -5.0 V and the second voltage pulse is about -10.0 V.

24. The method of claim 22, wherein the fourth time interval is between about $100\ \mu\text{sec}$ and about $300\ \mu\text{sec}$, the fifth time interval is between about 10
10 μsec and about $30\ \mu\text{sec}$ and the sixth time interval is between about $100\ \mu\text{sec}$ and about $300\ \mu\text{sec}$.

25. The method of claim 22, wherein the fourth time interval is about $200\ \mu\text{sec}$, the fifth time interval is about $20\ \mu\text{sec}$ and the sixth time interval is
15 about $200\ \mu\text{sec}$.

26. A method for erasing a semiconductor device comprising:
applying a constant positive voltage pulse for a first time interval at the source of the semiconductor device;
20 applying a first negative voltage pulse for a second time interval at the gate of the semiconductor device; and
applying a second negative voltage pulse for a third time interval at the gate of the semiconductor device;
wherein said second negative voltage pulse step is greater in
25 magnitude than said first negative voltage pulse step.

27. The method of claim 22, wherein the constant positive voltage is about 5.0 V.

30 28. The method of claim 22, wherein the first negative voltage pulse is about -5.0 V and the second negative voltage pulse is about -10.0 V.